AMENDMENT TO CLAIMS

1-11. (Cancelled)

12. (New) A circuit simulation method comprising the steps of:

(a) recognizing, from mask layout data for an integrated circuit, the shape of a first transistor portion which is provided in the integrated circuit;

(b) obtaining transistor size data and transistor model recognition data of the first transistor portion based on a result of the step of recognizing the shape of the first transistor portion;

(c) obtaining device measurement data by measuring an electrical characteristic of a device for measurement in which transistors each having a different stress are provided;

(d) recognizing, from the device measurement data, the shape of a second transistor portion which is provided in the device for measurement;

(e) extracting parameters based on a result of the step of recognizing the shape of the second transistor portion and converting the device measurement data into parameters having model parameter groups according to the stress;

(f) inputting as a netlist the transistor size data and the transistor model recognition data in a circuit simulator and inputting in the circuit simulator the parameters having the model parameter groups according to the stress; and

(g) selecting, using the circuit simulator, a parameter suitable for each of the transistors provided in the integrated circuit from among the parameters having the model parameter groups according to the stress to carry out a circuit simulation in consideration of a stress applied to each of the transistors.

13. (New) The circuit simulation method of claim 12, wherein the step (a) recognizes a width of a source/drain region extending, at one side, from one end of a gate electrode to an isolation region and a width of the isolation region, as the step of recognizing the shape of the first transistor portion.

14. (New) The circuit simulation method of claim 12, wherein the step (d) recognizes a width of a source/drain region extending, at one side, from one end of a gate electrode to an isolation region and a width of the isolation region, as the step of recognizing the shape of the second transistor portion.

15. (New) The circuit simulation method of claim 12, wherein in the step (b), the transistor size data includes a transistor size comprising a gate length and a gate width.

16. (New) The circuit simulation method of claim 12, wherein in the step (g), a most suitable model parameter is selected from among the model parameter groups in accordance with the stress to carry out the circuit simulation, even in a situation where transistors have a same size.

17. (New) The circuit simulation method of claim 12, wherein the transistors are each formed by a MIS transistor comprising a gate electrode, a gate insulating film, an active region and an isolation insulating film surrounding the active region;

wherein the step (c) at least includes a step of measuring items each serving as an index of the stress applied from the isolation insulating film to each of the MIS transistors; and

wherein the items, each serving as an index of the stress applied to each of the MIS transistors, include at least one of a position of the gate electrode in the active region, a size of the active region, and a width of the isolation insulating film.

18. (New) The circuit simulation method of claim 17, wherein the items, each serving as an index of the stress applied to the MIS transistors, further include at least one of a depth of the active region, a method for forming the isolation insulating film, a depth of the isolation insulating film, a material for use in forming the isolation insulating film, a size of the gate insulating film, and a material for use in forming the gate insulating film.

19. (New) The circuit simulation method of claim 12, wherein in the step (e), model parameter groups including additional models are prepared;

wherein in the step (f), the parameters having the model parameter groups including the additional models are input to the circuit simulator; and

wherein in the step (g), a correction is made using the additional models when selecting a parameter suitable for each of the transistors provided in the integrated circuit.

20. (New) The circuit simulation method of claim 12, wherein the method further comprises, after the steps (a) and (d) and prior to the step (g), the step of preparing a reference table including pieces of information for associating each of the transistors provided in the integrated circuit with the parameter that should be assigned to the each of the transistors based on the results of the step of recognizing the shape of the first transistor portion and the step of

recognizing the shape of the second transistor portion, and the step of inputting the reference table to the circuit simulator, and

wherein in the step (g), the selection of the parameter suitable for each of the transistors provided in the integrated circuit is automatically carried out using the reference table.

21. (New) The circuit simulation method of claim 20, wherein the reference table is used to associate each of the transistors provided in the integrated circuit with a plurality of weighted parameters.